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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,129	06/16/2000	Manfred Reithinger	00P7685US	2660

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/596,129	REITHINGER ET AL.
	Examiner	Art Unit
	Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 6-26* is/are pending in the application.

4a) Of the above claim(s) *8-10 and 14* is/are withdrawn from consideration.

5)☒ Claim(s) *11-13,15,17 and 21* is/are allowed.

6)☒ Claim(s) *1,6,7,16,18,20 and 22-26* is/are rejected.

7)☒ Claim(s) *3, 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 22-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitations of having "an electrical conductor" structure recited in base claims (claims 1, 6, 18, 20) formed on "a printed circuit board" as recited in new claims 22-26 are not supported by the original disclosure. In the other words, for example, the independent claim 1 recites an electrical conductor structure having an electrical conductor being elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer, such electrical conductor being electrically connected to the plurality of electrical contacts of the chips. However, such described electrical conductor structure above is disposed on "a semiconductor wafer", but not disposed on "a printed circuit board" as recited in the new claims 22-26.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitou et al (US. 5,739,546).

Saitou (Figs. 1 and 2) discloses a semiconductor, comprising: a semiconductor wafer having a plurality of integrated circuit chips 2 thereon, such chips being separated by "scribe line" separating regions 3 in the wafer, such wafer having a plurality of electrical contact pads 10; a dielectric member 7 having an electrical conductor 8 thereon, such electrical conductor 8 being elevated above the separating regions 3 in the fractional portion of the wafer, such electrical conductor 8 being electrically connected to the plurality of electrical contact pads 10 to electrically interconnect such plurality of chips, portions of the dielectric member 7 with portions of the electrical conductor 8 thereon spanning the regions in the wafer; and a plurality of voltage generator integrated circuits, each one being associated with, and disposed adjacent to, a corresponding one of the chips 2 (column 3, lines 19-22). It is noted that the dielectric member 7 is "a self-supporting dielectric member" because it is supports the electrical conductor 8.

4. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Murari et al (US. 5,696,404).

Murari (Figs. 2 and 5) discloses a semiconductor, comprising: a semiconductor wafer having a plurality of integrated circuit chips 2 thereon, such chips being separated by separating regions 11 in the wafer such wafer having a plurality of electrical contacts 6 and 7; a dielectric member 14 having the line bus 12 of electrical conductor 13 thereon (Fig. 5 and column 4, lines 11-20), such electrical conductor 13 or the bus line 12 being elevated above the regions in the fractional portion of the wafer, such electrical conductor 13 or the line bus 12 being electrically connected to the plurality of electrical

contacts 6 and 7 to electrically interconnect such plurality of chips, portions of the dielectric member 14 with portions of the electrical conductor 13 or the line bus 12 thereon spanning the regions in the wafer (see Fig. 2 and column 4, lines 11-20); and a plurality of voltage generators 3 and 4 including a plurality of different electrical components (Fig. 3B), each one being associated with, and disposed adjacent to, a corresponding one of the chips (column 3, lines 30-36). It is noted that the dielectric member 14 is "a self-supporting dielectric member" because it is supports the electrical conductor 13.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16, 18, 20, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitou et al or Murari et al in view of Barth et al (US. 6,233,184).

Neither Saitou nor Murari discloses the semiconductor wafer being a semiconductor package.

However, Barth (Fig. 3f) teaches the forming of a semiconductor wafer as a chip scale package 72 for connecting the membrane electrical conductor 20 to the electrical interconnect of the printed circuit board 74. Accordingly, it would have been obvious to connect the electrical conductor of Saitou or Murari to the printed circuit board for the

purpose of providing a fully tested package in wafer processing, so that the need for final module test after dicing is eliminated and the time and cost for testing and packaging is saved, as taught by Barth (column 9, lines 64-67).

Allowable Subject Matter

7. Claims 11-13, 15, 17 and 21 are allowed.

8. Claims 3 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all of the combination of the device structure as recited in the above claims, including the voltage generators being disposed in the separating region.

Response to Arguments

9. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PC
November 7, 2003

PHAT X. CAO
PRIMARY EXAMINER